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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/063,772	05/11/2002	Tsung-Yi Lin	VIAP0049USA	1061

27765 7590 10/18/2004

NAIPO (NORTH AMERICA INTERNATIONAL PATENT OFFICE)
P.O. BOX 506
MERRIFIELD, VA 22116

EXAMINER	
GUYTON, PHILIP A	
ART UNIT	**PAPER NUMBER**
2113	

DATE MAILED: 10/18/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/063,772	LIN ET AL.	
	Examiner	Art Unit	
	Philip Guyton	2113	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 May 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 2* is/are rejected.

7)☒ Claim(s) *3-5* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 May 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1 and 2 are rejected under 35 U.S.C. 103(a) as being unpatentable over Walker et al. (5,632,039) in view of Ranson (5,689,202).

Walker et al. disclose a method for determining an operating voltage of floating point error detection of a central processing unit (CPU) (Fig.1, item 101) through a control circuit (column 1, lines 64-67); said CPU comprising a first output port [voltage detect sense pin (column 2, lines 4-7 and Fig.2, VOLDET)], wherein said first output port is floating (column 2, lines 9-10) when said operating voltage of floating point error detection of said CPU is a certain value, and said first output port is connected to a grounding [driven low (column 2, lines 7-8)] when said operating voltage of floating point error detection of said CPU is another value; said control circuit comprising a test port [reference pin of voltage reference source (Fig.2, item 202)] connected to the first output

port of said CPU for determining said operating voltage of floating point error detection of said CPU; said method comprising:

providing a power supply (Fig.2, supply signal +5V above item 214) connected to the first output port of said CPU via a resistor (Fig.2, item 214) for supplying a first voltage level; and

measuring a voltage level at said test port of said control circuit to determine said operating voltage of floating point error detection of said CPU (column 4, lines 30-39 and lines 40-59).

Note that while Walker et al. do not disclose using this method to determine the operating voltage of floating point error detection, it is inherent that the voltage of floating point error will be equal to the operating voltage of the CPU.

Walker et al. fail to teach wherein said first output port is floating when said operating voltage of floating point error detection of said CPU is higher than a first predetermined voltage level, and said first output port is connected to a grounding when said operating voltage of floating point error detection of said CPU is lower than said first predetermined voltage level.

Ranson teaches a signaling environment with two possible voltage levels (column 2, lines 7-13), where the output signal [first output port] is driven low when the voltage [operating voltage of floating point error detection] is less than a reference voltage [first predetermined voltage level], and the output signal is high when the voltage is greater than a reference voltage (column 5, lines 40-50).

Walker et al. and Ranson are analogous art because they are from the same field of endeavor, namely, determination of voltage in a computer system.

At the time the invention was made it would have been obvious to a person of ordinary skill in the art to modify Walker et al. with the teachings of Ranson. A person of ordinary skill in the art would have been motivated to do so to enable all of the functions to be generated internally to the control circuit, as taught by Ranson (column 2, lines 60-66).

With respect to claim 2, Ranson discloses wherein said first voltage level is a positive voltage, said operating voltage of said CPU is higher than said first predetermined voltage level when said voltage level at said test port of said control circuit is higher than a second predetermined voltage level [when supply is 5V, OUT is driven high (column 5, lines 42-45)], and said operating voltage of said CPU is lower than said first predetermined voltage level when said voltage level at said test port of said control circuit is lower than said second predetermined voltage level [when supply is 3.3V, OUT is driven low (column 5, lines 40-42)].

Allowable Subject Matter

4. Claims 3-5 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. See PTO-892 attached.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Philip Guyton whose telephone number is (703) 305-4669, and will change to (571) 272-3807 beginning 10/13/04. The examiner can normally be reached on M-F 8:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on (703) 305-9713. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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